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HP/NSD

<p>HITACHI SEMICONDUCTOR TECHNICAL REPORT</p>
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HB54A5129F1-10B Data Sheet

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# HB54A5129F1-10B

512 MB Registered DDR SDRAM DIMM  
64-Mword  $\times$  72-bit, 1-Bank Module  
(18 pcs of 64 M  $\times$  4 Components)

## HITACHI

ADE-203-1159 (Z)  
Preliminary  
Rev. 0.0  
Feb. 7, 2000

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### Description

The HB54A5129F1 is a 64M  $\times$  72  $\times$  1-bank Double Data Rate (DDR) SDRAM Module, mounted 18 pieces of 256-Mbit DDR SDRAM (HM5425401BTT) sealed in TSOP package, 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). Read and write operations are performed at the cross points of the CK and the  $\overline{\text{CK}}$ . This high speed data transfer is realized by the 2-bit prefetch pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

### Features

- 184-pin socket type package (dual lead out)
  - Outline: 133.35 mm (Length)  $\times$  43.18 mm (Height)  $\times$  4.00 mm (Thickness)
  - Lead pitch: 1.27 mm
- 2.5 V power supply ( $V_{\text{CC}}/V_{\text{CCQ}}$ )
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 100 MHz (max)
- Data inputs and outputs are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2/4/8
  - Burst read stop capability

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.



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## HB54A5129F1-10B

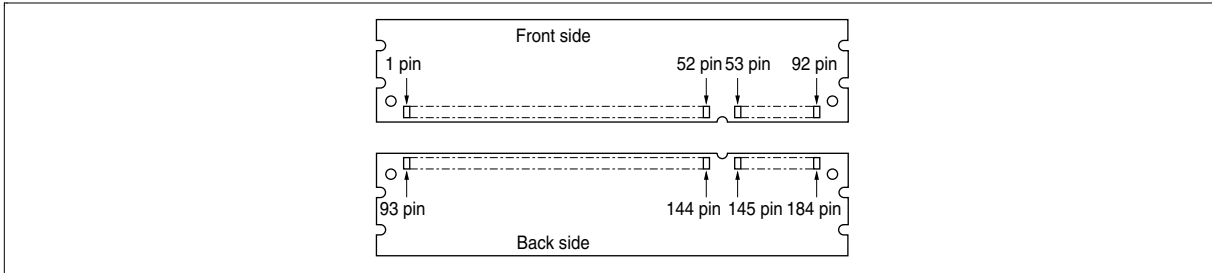
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- Programmable burst sequence
  - Sequential
  - Interleave
- Start addressing capability
  - Even and Odd
- $\overline{\text{CAS}}$  latency: 3
- 8192 refresh cycles: 7.8  $\mu\text{s}$  (8192 row/64 ms)
- 2 variations of refresh
  - Auto refresh
  - Self refresh

### Ordering Information

Type No.	Frequency	$\overline{\text{CAS}}$ latency	Package	Contact pad
HB54A5129F1-10B	100 MHz	3	184-pin dual lead out socket type	Gold

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**Pin Arrangement**


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V <sub>REF</sub>	47	DQS8	93	V <sub>SS</sub>	139	V <sub>SS</sub>
2	DQ0	48	A0	94	DQ4	140	DM8/DQS17
3	V <sub>SS</sub>	49	CB2	95	DQ5	141	A10
4	DQ1	50	V <sub>SS</sub>	96	V <sub>CCQ</sub>	142	CB6
5	DQS0	51	CB3	97	DM0/DQS9	143	V <sub>CCQ</sub>
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V <sub>CC</sub>	53	DQ32	99	DQ7	145	V <sub>SS</sub>
8	DQ3	54	V <sub>CCQ</sub>	100	V <sub>SS</sub>	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	$\overline{\text{RESET}}$	56	DQS4	102	NC	148	V <sub>CC</sub>
11	V <sub>SS</sub>	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	V <sub>SS</sub>	104	V <sub>CCQ</sub>	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V <sub>SS</sub>
15	V <sub>CCQ</sub>	61	DQ40	107	DM1/DQS10	153	DQ44
16	NC	62	V <sub>CCQ</sub>	108	V <sub>CC</sub>	154	$\overline{\text{RAS}}$
17	NC	63	$\overline{\text{WE}}$	109	DQ14	155	DQ45
18	V <sub>SS</sub>	64	DQ41	110	DQ15	156	V <sub>CCQ</sub>
19	DQ10	65	$\overline{\text{CAS}}$	111	NC	157	$\overline{\text{S0}}$
20	DQ11	66	V <sub>SS</sub>	112	V <sub>CCQ</sub>	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	V <sub>CCQ</sub>	68	DQ42	114	DQ20	160	V <sub>SS</sub>
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V <sub>CC</sub>	116	V <sub>SS</sub>	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

## HB54A5129F1-10B

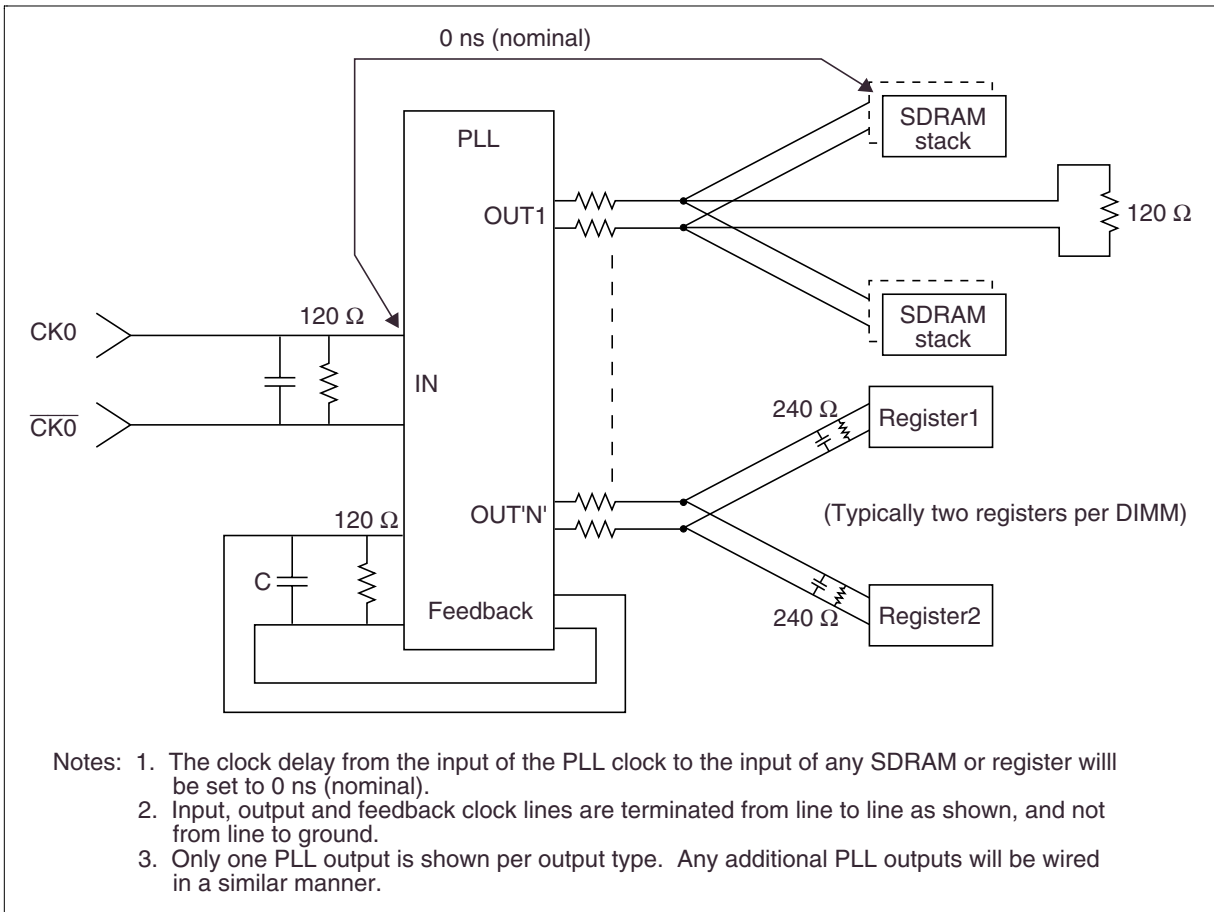
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V <sub>SS</sub>	72	DQ48	118	A11	164	V <sub>CCQ</sub>
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	V <sub>SS</sub>	120	V <sub>CC</sub>	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V <sub>CCQ</sub>	76	NC	122	A8	168	V <sub>CC</sub>
31	DQ19	77	V <sub>CCQ</sub>	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	V <sub>SS</sub>	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V <sub>SS</sub>	80	DQ51	126	DQ28	172	V <sub>CCQ</sub>
35	DQ25	81	V <sub>SS</sub>	127	DQ29	173	NC
36	DQS3	82	V <sub>CCID</sub>	128	V <sub>CCQ</sub>	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	V <sub>CC</sub>	84	DQ57	130	A3	176	V <sub>SS</sub>
39	DQ26	85	V <sub>CC</sub>	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	V <sub>SS</sub>	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V <sub>SS</sub>	88	DQ59	134	CB4	180	V <sub>CCQ</sub>
43	A1	89	V <sub>SS</sub>	135	CB5	181	SA0
44	CB0	90	WP	136	V <sub>CCQ</sub>	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V <sub>CC</sub>	92	SCL	138	$\overline{\text{CK0}}$	184	V <sub>CCSPD</sub>

**Pin Description**

<b>Pin name</b>	<b>Function</b>
A0 to A12	Address input — Row address      A0 to A12 — Column address    A0 to A9, A11
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
$\overline{\text{RAS}}$	Row address strobe command
$\overline{\text{CAS}}$	Column address strobe command
$\overline{\text{WE}}$	Write enable
$\overline{\text{S0}}$	Chip select
CKE0	Clock enable
CK0	Clock input
$\overline{\text{CK0}}$	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8/DQS9 to DQS17	Input and output data strobe
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
WP	Write protect for serial PD
SA0 to SA2	Serial address input
$V_{\text{CC}}$	Power for internal circuit
$V_{\text{CCQ}}$	Power for DQ circuit
$V_{\text{CCSPD}}$	Power for serial EEPROM
$V_{\text{REF}}$	Input reference voltage
$V_{\text{SS}}$	Ground
$V_{\text{CCID}}$	$V_{\text{CC}}$ indentation flag
$\overline{\text{RESET}}$	Reset pin (forces register inputs low)
NC	No connection



Differential Clock Net Wiring (CK0,  $\overline{\text{CK0}}$ )



## Pin Functions (1)

**CK (CLK),  $\overline{\text{CK}}$  ( $\overline{\text{CLK}}$ ) (input pin):** The CK and the  $\overline{\text{CK}}$  are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the  $V_{\text{REF}}$  level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the  $\overline{\text{CK}}$ . When a write operation, DMs and DQs are referred to the cross point of the DQS and the  $V_{\text{REF}}$  level. DQSs for write operation are referred to the cross point of the CK and the  $\overline{\text{CK}}$ .

**$\overline{\text{S}}$  ( $\overline{\text{CS}}$ ) (input pin):** When  $\overline{\text{S}}$  is Low, commands and data can be input. When  $\overline{\text{S}}$  is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

**$\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and  $\overline{\text{WE}}$  (input pins):** These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

**A0 to A12 (input pins):** Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the  $V_{\text{REF}}$  level in a bank active command cycle. Column address (AY0 to AY9, AY11) is loaded via the A0 to the A9, the A11 at the cross point of the CK rising edge and the  $V_{\text{REF}}$  level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

**A10 (AP) (input pin):** A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

**BA0/BA1 (input pin):** BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

**CKE (input pin):** CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CK cycle ( $= L_{\text{CKEPW}}$ ) at least, that is, if CKE changes at the cross point of the CK rising edge and the  $V_{\text{REF}}$  level with proper setup time  $t_{\text{IS}}$ , at the next CK rising edge CKE level must be kept with proper hold time  $t_{\text{IH}}$ .

## **Pin Functions (2)**

**DQ, CB (input and output pins):** Data are input to and output from these pins.

**DQS (input and output pin):** DQS provide the read data strobes (as output) and the write data strobes (as input).

**V<sub>CC</sub> and V<sub>CCQ</sub> (power supply pins):** 2.5 V is applied. (V<sub>CC</sub> is for the internal circuit and V<sub>CCQ</sub> is for the output buffer.)

**V<sub>CCSPD</sub> (power supply pin):** 2.5 V is applied (For serial EEPROM).

**V<sub>SS</sub> (power supply pin):** Ground is connected.

**$\overline{\text{RESET}}$  (input pin):** LVCMOS reset input. When  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are low.

## **Detailed Operation Part and Timing Waveforms**

Refer to the HM5425161B/HM5425801B/HM5425401B Series datasheet. DM pins of component device fixed to V<sub>SS</sub> level on the module board. DIMM  $\overline{\text{CAS}}$  latency = Device CL + 1 for registered type.

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +4.6	V	1
Supply voltage relative to $V_{SS}$	$V_{CC}, V_{CCQ}$	-1.0 to +4.6	V	1
Short circuit output current	$I_{out}$	50	mA	
Power dissipation	$P_T$	18	W	
Operating temperature	$T_{opr}$	0 to +55	°C	
Storage temperature	$T_{stg}$	-50 to +100	°C	

Note: 1. Respect to  $V_{SS}$

### DC Operating Conditions ( $T_a = 0$ to $+55^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}, V_{CCQ}$	2.3	2.5	2.7	V	1, 2
	$V_{SS}$	0	0	0	V	
Input reference voltage	$V_{REF}$	1.15	1.25	1.35	V	1
Termination voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	1
DC Input high voltage	$V_{IH}$	$V_{REF} + 0.18$	—	$V_{CCQ} + 0.3$	V	1, 3
DC Input low voltage	$V_{IL}$	-0.3	—	$V_{REF} - 0.18$	V	1, 4
DC Input signal voltage	$V_{IN}$ (dc)	-0.3	—	$V_{CCQ} + 0.3$	V	5
DC differential input voltage	$V_{SWING}$ (dc)	0.36	—	$V_{CCQ} + 0.6$	V	6

Notes: 1. All parameters are referred to  $V_{SS}$ , when measured.

2.  $V_{CCQ}$  must be lower than or equal to  $V_{CC}$ .

3.  $V_{IH}$  is allowed to exceed  $V_{CC}$  up to 4.6 V for the period shorter than or equal to 5 ns.

4.  $V_{IL}$  is allowed to outreach below  $V_{SS}$  down to -1.0 V for the period shorter than or equal to 5 ns.

5.  $V_{IN}$  (dc) specifies the allowable dc execution of each differential input.

6.  $V_{SWING}$  (dc) specifies the input differential voltage required for switching.

**DC Characteristics** ( $T_a = 0$  to  $+55^\circ\text{C}$ ,  $V_{CC}$ ,  $V_{CCQ} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	HB54A5129F1		Unit	Test conditions	Notes
		-10B				
		Min	Max			
Operating current (ACTV-PRE)	$I_{CC0}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $t_{RC} = \text{min}$	1, 2, 5
Operating current (ACTV-READ-PRE)	$I_{CC1}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $\text{BL} = 2$ , $\text{CL} = 3.5$ , $t_{RC} = \text{min}$	1, 2, 5
Idle power down standby current	$I_{CC2P}$	—	TBD	mA	$\text{CKE} \leq V_{IL}$	4
Idle standby current	$I_{CC2N}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $\overline{\text{CS}} \geq V_{IH}$	4
Active power down standby current	$I_{CC3P}$	—	TBD	mA	$\text{CKE} \leq V_{IL}$	3
Active standby current	$I_{CC3N}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $t_{RAS} = \text{max}$	3
Operating current (Burst read operation)	$I_{CC4R}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $\text{BL} = 2$ , $\text{CL} = 3.5$	1, 2, 5, 6
Operating current (Burst write operation)	$I_{CC4W}$	—	TBD	mA	$\text{CKE} \geq V_{IH}$ , $\text{BL} = 2$ , $\text{CL} = 3.5$	1, 2, 5, 6
Auto refresh current	$I_{CC5}$	—	TBD	mA	$t_{RFC} = \text{min}$ , Input $\leq V_{IL}$ or $\geq V_{IH}$	
Self refresh current	$I_{CC6}$	—	TBD	mA	Input $\geq V_{CC} - 0.2\text{ V}$ Input $\leq 0.2\text{ V}$	
Input leakage current	$I_{LI}$	-10	10	$\mu\text{A}$	$V_{CC} \geq V_{in} \geq V_{SS}$	
Output leakage current	$I_{LO}$	-10	10	$\mu\text{A}$	$V_{CC} \geq V_{out} \geq V_{SS}$	
Output high voltage	$V_{OH}$	$V_{TT} + 0.76$	—	V	$I_{OH}(\text{max}) = -15.2\text{ mA}$	
Output low voltage	$V_{OL}$	—	$V_{TT} - 0.76$	V	$I_{OL}(\text{min}) = 15.2\text{ mA}$	

- Notes.
1. These  $I_{CC}$  data are measured under condition that DQ pins are not connected.
  2. One bank operation.
  3. One bank active.
  4. All banks idle.
  5. Command/Address transition once per one cycle.
  6. Data/Data mask transition twice per one cycle.
  7. The  $I_{CC}$  data on this table are measured with regard to  $t_{CK} = \text{min}$  in general.

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**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC}$ ,  $V_{CCQ} = 2.5\text{ V} \pm 0.2\text{ V}$ )

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	TBD	TBD	pF	1
Input capacitance (Command)	$C_{i2}$	TBD	TBD	pF	1
Data and DQS input/output capacitance (I/O)	$C_o$	TBD	TBD	pF	1, 2

Notes: 1. These parameters are measured on conditions:  $f = 100\text{ MHz}$ ,  $V_{out} = V_{CCQ}/2$ ,  $\Delta V_{out} = 0.2\text{ V}$ .  
2. Dout circuits are disabled.

**AC Characteristics** ( $T_a = 0\text{ to }+55^\circ\text{C}$ ,  $V_{CC}$ ,  $V_{CCQ} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	HB54A5129F1		Unit	Notes
		Min	Max		
System clock cycle time	$t_{CK}$	10	15	ns	10
Input clock high level time	$t_{CH}$	TBD	—	$t_{CK}$	
Input clock low level time	$t_{CL}$	TBD	—	$t_{CK}$	
CLK to DQS skew	$t_{DQSK}$	TBD	TBD	ns	2
DATA to CLK skew	$t_{AC}$	TBD	TBD	ns	2
Dout to DQS skew	$t_{DQSQ}$	-0.6	0.6	ns	3
Dout/DQS valid window	$t_{DV}$	0.35	—	$t_{CK}$	4
DQS valid window	$t_{DQSV}$	0.35	—	$t_{CK}$	4
DQS read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	
DQS read postamble	$t_{RPST}$	0.4	0.6	$t_{CK}$	
Dout-High impedance delay from $\text{CLK}/\overline{\text{CLK}}$	$t_{HZ}$	TBD	TBD	ns	5
Dout-Low impedance delay from $\text{CLK}/\overline{\text{CLK}}$	$t_{LZ}$	TBD	TBD	ns	6
DQ input pulse width	$t_{DIPW}$	2	—	ns	7
Data to data strobe setup time	$t_{DS}$	0.6	—	ns	8
Data to data strobe hold time	$t_{DH}$	0.6	—	ns	8
Clock to DQS write preamble setup time	$t_{WPRES}$	TBD	—	ns	
Clock to DQS write preamble hold time	$t_{WPREH}$	TBD	—	$t_{CK}$	
DQS last edge to High-Z time (DQS write postamble)	$t_{WPST}$	0.4	0.6	$t_{CK}$	9
Clock to the DQS first rising edge for write delay	$t_{DQSS}$	TBD	TBD	$t_{CK}$	

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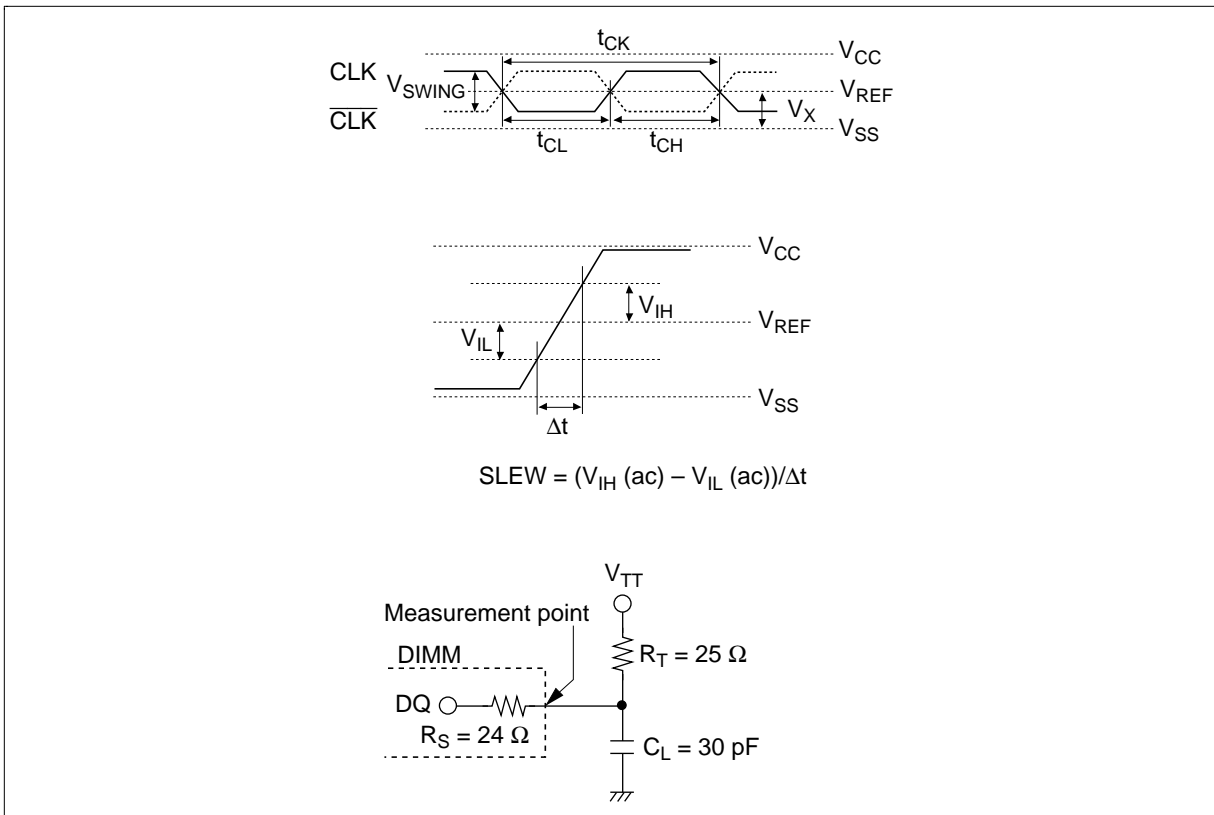
Parameter	Symbol	HB54A5129F1		Unit	Notes
		-10B			
		Min	Max		
DQS falling edge to CLK setup time	$t_{DSS}$	TBD	—	$t_{CK}$	
DQS falling edge hold time to CLK	$t_{DSH}$	TBD	—	$t_{CK}$	
DQS high pulse width (DQS write)	$t_{DQSH}$	0.35	—	$t_{CK}$	
DQS low pulse width (DQS write)	$t_{DQSL}$	0.35	—	$t_{CK}$	
Input command and address setup time	$t_{IS}$	TBD	—	ns	8
Input command and address hold time	$t_{IH}$	TBD	—	ns	8
Active command period	$t_{RC}$	70	—	ns	
Auto refresh to active/Auto refresh command cycle	$t_{RFC}$	80	—	ns	
Active to Precharge command period	$t_{RAS}$	50	120000	ns	
Active to column command period	$t_{RCD}$	20	—	ns	
Last data in to precharge	$t_{WR}$	TBD	—	ns	
Precharge to active command period	$t_{RP}$	20	—	ns	
Active to active command period	$t_{RRD}$	15	—	ns	
Average periodic refresh interval	$t_{REF}$	—	7.8	$\mu$ s	

- Notes.
1. On all AC measurements, we assume the test conditions shown in the next page. For timing parameter definitions, see 'Timing Waveforms' section.
  2. This parameter defines the signal transition delay from the cross point of CLK and  $\overline{CLK}$ . The signal transition is defined to occur when the signal level crossing  $V_{TT}$ .
  3. The timing reference level is  $V_{TT}$ .
  4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing  $V_{TT}$ .
  5.  $t_{HZ}$  is defined as Dout transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CLK and  $\overline{CLK}$ . This parameter is not referred to a specific Dout voltage level, but specify when the device output stops driving.
  6.  $t_{LZ}$  is defined as Dout transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific Dout voltage level, but specify when the device output begins driving.
  7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing  $V_{REF}$ .
  8. The timing reference level is  $V_{REF}$ .
  9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
  10.  $t_{CK}$  max is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
  11.  $V_{CC}$  is assumed to be  $2.5\text{ V} \pm 0.2\text{ V}$ .  $V_{CC}$  power supply variation per cycle expected to be less than  $0.4\text{ V}/400\text{ cycle}$ .

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## Test Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input reference voltage	$V_{REF}$	1.15	1.25	1.35	V
Termination voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
AC input high voltage	$V_{IH} (ac)$	$V_{REF} + 0.35$	—	—	V
AC input low voltage	$V_{IL} (ac)$	—	—	$V_{REF} - 0.35$	V
AC differential input high voltage	$V_{SWING} (ac)$	0.7	—	$V_{CCQ} + 0.6$	V
AC differential cross point voltage	$V_X (ac)$	$V_{REF} - 0.2$	$V_{REF}$	$V_{REF} + 0.2$	V
Input signal slew rate	SLEW	—	1	—	V/ns

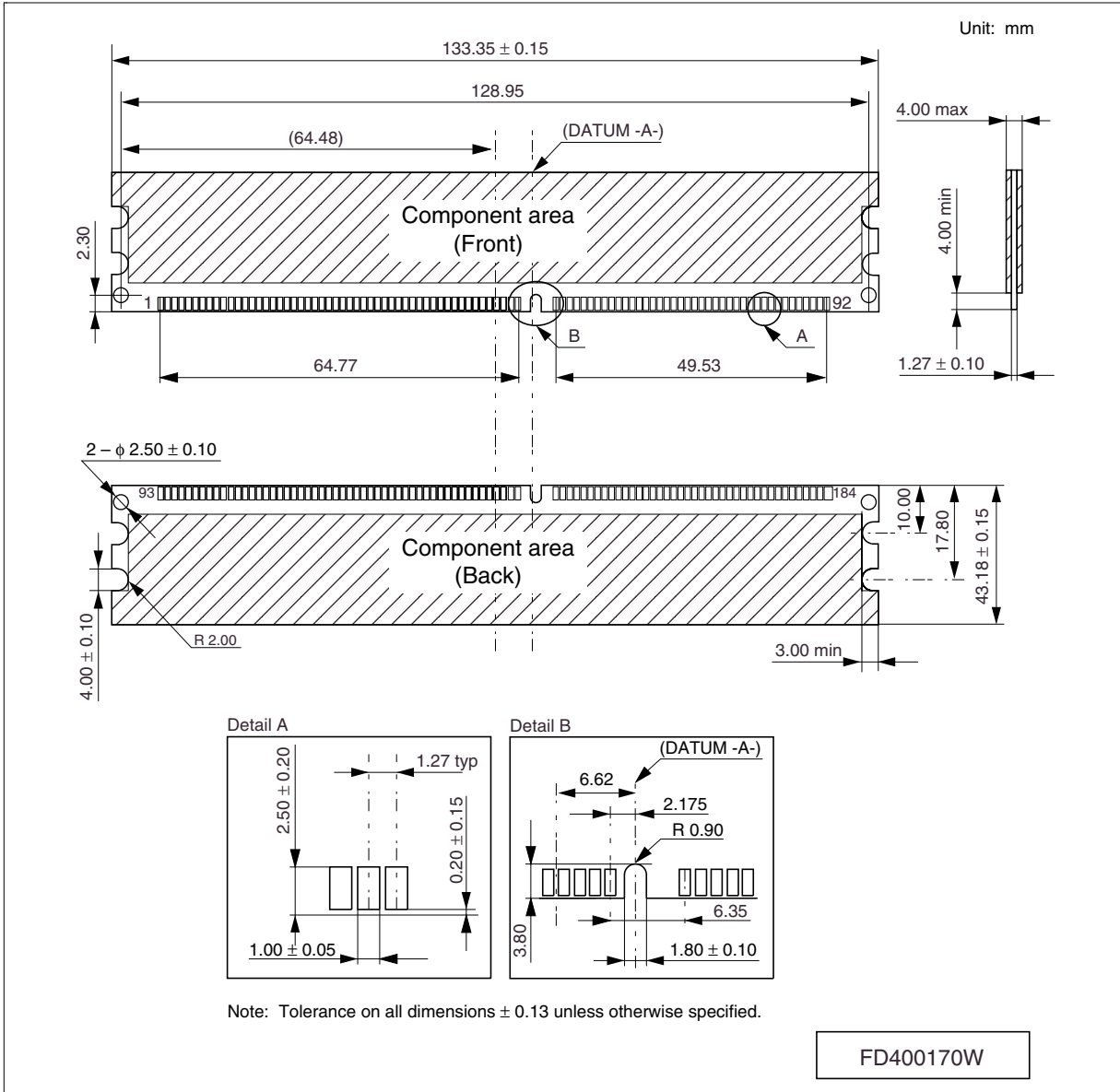


**Timing Parameter Measured in Clock Cycle for Registered DIMM**

Parameter	Symbol	Number of clock cycle	
		Min	Max
Write to pre-charge command delay (same bank)	$t_{WPD}$	3 + BL/2	
Read to pre-charge command delay (same bank)	$t_{RPD}$	BL/2	
Write to read command delay (to input all data)	$t_{WRD}$	2 + BL/2	
Burst stop command to write command delay	$t_{BSTW}$	2	
Burst stop command to DQ High-Z	$t_{BSTZ}$	3	
Read command to write command delay (to output all data)	$t_{RWD}$	2 + BL/2	
Pre-charge command to High-Z	$t_{HZP}$	3	
Write command to data in latency	$t_{WCD}$	2	
Write recovery	$t_{WR}$	1	
Register set command to active or register set command	$t_{MRD}$	2	
Self refresh exit to non-read command	$t_{SNR}$	10	
Self refresh exit to read command	$t_{SRD}$	200	
Power down entry	$t_{PDEN}$		1
Power down exit to command input	$t_{PDEX}$		1
CKE minimum pulse width	$t_{CKEPW}$	1	

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## Physical Outline



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